OM1400A-105
14 Bit, 105 MSPS ADC Module

Analog-to-Digital Converter Module with Turbolinear™ Technology

Description

The OM1400A-105 is a high-speed and high-performance analog-to-digital converter module optimized to achieve exceptionally high linearity when digitizing signals at very high IF. The module has a maximum sampling rate of 105 MSPS and is primarily built around Optichron's Linearizer with Turbolinear™ technology in addition to a 14-bit AD6645 analog-to-digital converter, and an AD8351 buffer amplifier, which provides a buffered, single-ended, 50 ohm input. The module output is a digitized signal optimized for up to 25 dB improvement in SFDR when sub-sampling signals in the 2nd, 3rd, and 4th Nyquist Zones.

The OM1400A-105 is targeted at a wide variety of applications requiring high linearity.

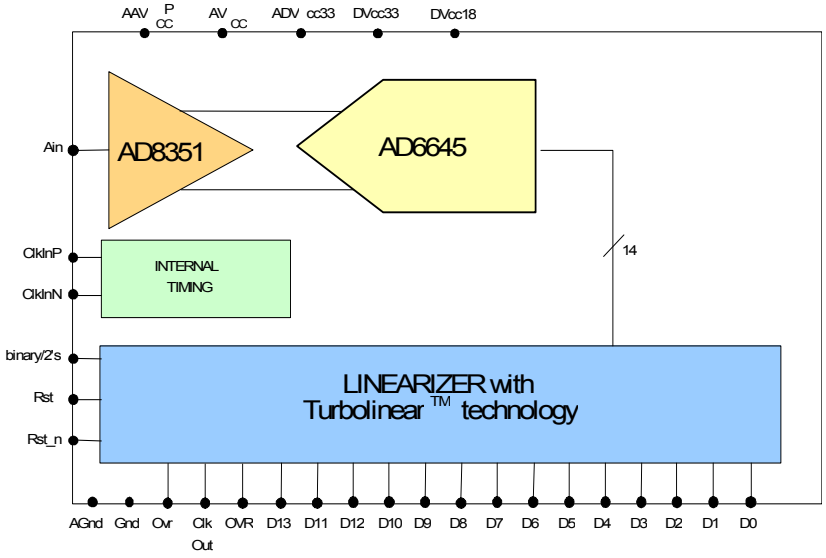
Applications

- Multi-channel, multi-mode receivers
- Base station transceiver
- Communications instrumentation
- Test and measurement
- Radar, infrared imaging
- High-resolution medical imaging
- Power amplifier linearization
- Software defined radio

Features

- 14-bit resolution, 105 MSPS sampling rate
- IF sampling to 205 MHz
- SFDR: 90dBc typical for one-tone 105-145 MHz f_{IN} measured at -1 dBFS peak amplitude
- SNR: 70 dBFS typical for one-tone 105-145 MHz f_{IN} measured at -1 dBFS peak amplitude
- 5dBm full-scale input power
- Single-ended, 50-ohm analog input buffer
- Selectable 2s complement or binary outputs
- 3.3V CMOS compatible
- Output clock for data output latching
- Module power dissipation: 2.8W
- BGA footprint

Module Block Diagram



PRELIMINARY DATA SHEET

Revision 0.4, June 2006
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Absolute Maximum Ratings

Absolute maximum ratings are over operating free-air temperature range unless otherwise noted.

Table 1: Absolute Maximum Ratings

Parameter	Min	Max	Units
Electrical			
Analog Input Voltage		6	V
Digital Core Voltage		2	V
Digital I/O		3.6	V
Digital Output Current		30	mA
Analog Core Voltage		6	V
Environmental			
Junction Temperature		+125	°C
Operating Temperature Range	-10	+85	°C
Storage Temperature Range	-50	+150	°C

Caution: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only; functional operation of the device at these or other conditions beyond those in the operational section of this specification is not implied.

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DC Specifications

(Typical, min, max values at T = 25°C, AAV_{CC} = AV_{CC} = 5V, DV_{CC33} = DV_{CCF33} = 3.3V, DV_{CC18} = 1.8V; sampling rate = 105 MSPS with 50% clock duty cycle with -1dBFS analog signal input unless otherwise noted.)

Table 2: DC Specifications

Parameter	Notes	Min	Typical	Max	Units
Resolution			14		Bits
Accuracy					
No Missing Codes			Guaranteed		
Offset Error		-75		+75	LSB
Offset Error Drift			1.5		ppm/°C
Analog Input					
Input Voltage Range Fullscale			1.1		Vp-p
Input Return Loss	50 ohm system		20		dB
Analog 5.0V Supply Voltage[a]	AV_{CC}, AAV_{CCP}	4.75	5.00	5.25	V
Analog 5.0V Supply Current	Total		303	352	mA
	AAV_{CCP} Supply		28	32	mA
	AV_{CC} Supply		275	320	mA
Digital 3.3V Supply Voltage[b]	$DV_{CC33}DV_{CCF33}$	3.0	3.3	3.6	V
Digital 3.3V Supply Current	Total		106	137	mA
Total	DV_{CC33} Supply		106	119	mA
Flash Read Operation	DV_{CCF33} Supply		14	18	mA
Flash Stand-by	DV_{CCF33} Supply		0.025	0.05	mA
Digital 1.8V Supply Voltage	DV_{CC18}	1.72	1.80	1.88	V
Digital 1.8V Supply Current			500	650	mA
Module					
Power Dissipation			2.8		W
Digital Core Power			900		mW

a. Optimal performance is achieved by keeping the analog supply voltage within 1% of 5.00V.

b. Optimal performance is achieved by keeping the digital supply voltage within 5% of 3.30V.

Digital Specifications

(AAV_{CC} = AV_{CC} = 5V, DV_{CC33} = DV_{CCF33} = 3.3V, DV_{CC18} = 1.8V; TMIN and TMAX at rated speed grade unless otherwise noted.)

Table 3: Digital Specifications

Parameter (Conditions)	Notes	Minimum	Typical	Maximum	Units
Logic Inputs					
Logic 1 Voltage		2.2		3.6	V
Logic 0 Voltage		0.0		1.0	V
Logic Outputs					V
Logic Compatibility			CMOS		
Logic 1 Voltage (DV_{CC} = 3.3V)		2.7		3.6	V
Logic 0 Voltage (DV_{CC} = 3.3V)		0.0		0.5	V

Switching Specifications

(AAV_{CC} = AV_{CC} = 5V, DV_{CC33} = DV_{CCF33} = 3.3V, DV_{CC18} = 1.8V; CLOAD 10 pF)

Table 4: Switching Specifications

Parameter (Conditions)	Name	Minimum	Typical	Maximum	Units
Conversion Rate [a]					MSPS
OM1400A-1050NZx		100		105	
OM1400A-1000NZx		95		100	
OM1400A-0950NZx		90		95	
OM1400A-0900NZx		85		90	
ClkInP, ClkInN Inputs					
Differential Input Voltage[b]		0.4			Vp-p
Differential Input Resistance			10		kΩ (kOhm)
Differential Input Capacitance			2.5		pF
ClkInP, ClkInN Input Parameters					
Clock Period[c]	t_{CIN}		10.0	1000	ns
Clock Pulsewidth High	t_{CINHI}	4.0	5.0		ns
Clock Pulsewidth Low	t_{CINLO}	4.0	5.0		ns
50% Duty Cycle for Optimum Performance					
ClkOut/DATA (D13:0)					
ClkOut Rising to DATA (Hold Time)	t_{H_CLKOUT}	2.0			ns
ClkOut Rising to DATA (Setup Time)	t_{S_CLKOUT}	2.0			ns
Latency			55		clocks
Aperture Delay t_A			-500		ps
Aperture Jitter			0.1		ps rms

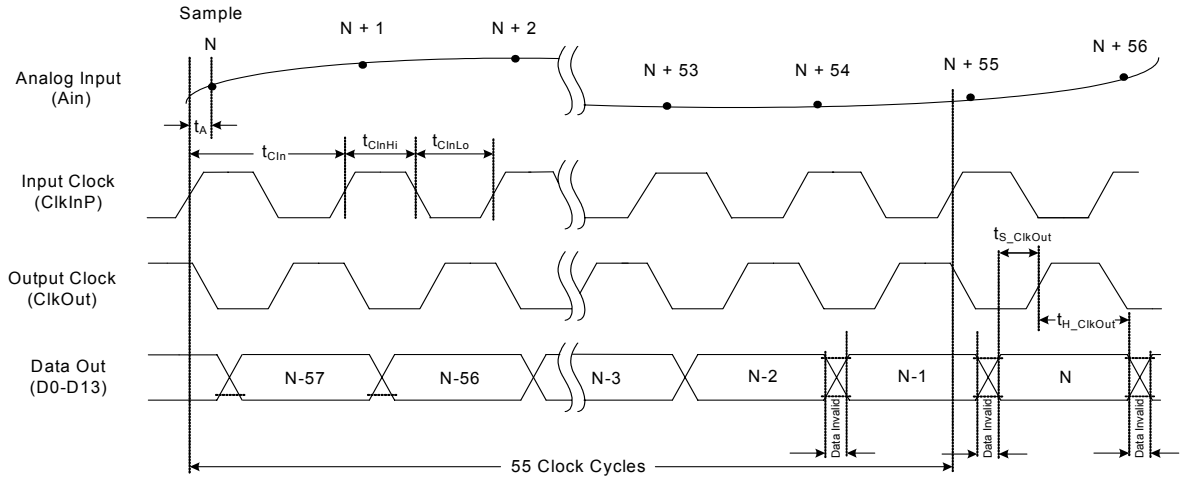
a. The ‘x’ in NZx refers to the Nyquist zone versions 2, 3, or 4 of the product. Each part number is calibrated at the maximum listed specification where the best performance is obtained. It is highly recommended that the module is operated at that rate. For a complete part number listing, see Ordering Guide on page 26.

b. Refer to the Applications Information “Clock Input” section on page 17 for optimal clocking conditions.

c. If the maximum clock period is exceeded or if the minimum pulsewidth is exceeded, the reset signal must be asserted.

Timing Diagram

Figure 1. Timing Diagram



AC Specifications

Table 5: Nyquist Zone 2 (52.5-105 MHz, Temp = 25°C, fs = 105 MSPS)

Parameter (Conditions)	Notes	Minimum	Typical	Maximum	Units
SNR (input at −1 dBFS)					
f_{IN} = fmin + 5%fs			70		dB
f_{IN} = (fmax + fmin)/2			70		dB
f_{IN} = fmax – 5%fs			70		dB
SINAD (input at −1 dBFS)					
f_{IN} = fmin + 5%fs			70		dB
f_{IN} = (fmax + fmin)/2			70		dB
f_{IN} = fmax – 5%fs			70		dB
SFDR (input at −1 dBFS)					
f_{IN} = fmin + 5%fs			92		dBFS
f_{IN} = (fmax + fmin)/2			91		dBFS
f_{IN} = fmax – 5%fs			90		dBFS
Two Tone IMD (F1, F2 at −7 dBFS)					
f_{IN} = {(fmax + fmin)/2} – 4.9 MHz {(fmax + fmin)/2} + 6.1 MHz			TBD		dBFS
Two Tone SFDR					
f_{IN} = {(fmax + fmin)/2} – 4.9 MHz {(fmax + fmin)/2} + 6.1 MHz			TBD		dB
Analog Input Bandwidth			270		MHz
Accuracy					
Gain Error			TBD	TBD	dB
Gain Error Drift			TBD		ppm/°C
Power Supply Rejection					
5.0V Supply			TBD		dB/V
3.3V Supply			TBD		dB/V

Note: ‘fs’ is the sampling rate.
fmax = fs
fmin = fs/2

Table 6: Nyquist Zone 3 (105-157.5 MHz, Temp = 25°C, fs = 105 MSPS)

Parameter (Conditions)	Notes	Minimum	Typical	Maximum	Units
SNR (one-tone input at −1 dBFS)					
f_{IN} = fmin + 5%fs			70		dB
f_{IN} = (fmax + fmin)/2			70		dB
f_{IN} = fmax – 5%fs			69		dB
SINAD (input at −1 dBFS)					
f_{IN} = fmin+5%fs			70		dB
f_{IN} = (fmax + fmin)/2			70		dB
f_{IN} = fmax – 5%fs			69		dB
SFDR (one-tone input at −1 dBFS)					
f_{IN} = fmin + 5%fs			87		dBc
f_{IN} = (fmax + fmin)/2			87		dBc
f_{IN} = fmax – 5%fs			87		dBc
Two Tone IMD (F1, F2 at −7 dBFS)					
f_{IN} =129.8757MHz; 152.347MHz			85		dBFS
Two Tone SFDR					
f_{IN} = 126.349686MHz; 137.349686MHz -100dBFS<Ain<-2dBFS			95		dB
Analog Input Bandwidth			270		MHz
Accuracy					
Gain Error		-0.9	0	0.7	dB
Gain Error Drift			TBD		ppm/°C
Power Supply Rejection					
5.0V Supply			0.37		dB/V
3.3V Supply			0.007		dB/V

Note: 'fs' is the sampling rate.
fmax = 3fs/2
fmin = fs

Table 7: Nyquist Zone 4 (157.5-210 MHz, Temp = 25°C, fs = 105 MSPS)

Parameter (Conditions)	Notes	Minimum	Typical	Maximum	Units
SNR (input at −1 dBFS)					
f_{IN} = fmin + 5%fs			69		dB
f_{IN} = (fmax + fmin)/2			69		dB
f_{IN} = fmax – 5%fs			68		dB
SINAD (input at −1 dBFS)					
f_{IN} = fmin+5%fs			TBD		dB
f_{IN} = (fmax + fmin)/2			TBD		dB
f_{IN} = fmax – 5%fs			TBD		dB
SFDR (input at −1 dBFS)					
f_{IN} = fmin + 5%fs			87		dBc
f_{IN} = (fmax + fmin)/2			85		dBc
f_{IN} = fmax – 5%fs			85		dBc
Two Tone IMD (F1, F2 at −7 dBFS)					
f_{IN} = {(fmax + fmin)/2} – 4.9 MHz {(fmax + fmin)/2} + 6.1 MHz			TBD		dBFS
Two Tone SFDR					
f_{IN} = {(fmax + fmin)/2} – 4.9 MHz {(fmax + fmin)/2} + 6.1 MHz			TBD		dB
Analog Input Bandwidth			270		MHz
Accuracy					
Gain Error			TBD	TBD	dB
Gain Error Drift			TBD		ppm/°C
Power Supply Rejection					
5.0V Supply			TBD		dB/V
3.3V Supply			TBD		dB/V

Note: 'fs' is the sampling rate.
fmax=2fs
fmin=3fs/2

Typical Performance Characteristics (Nyquist Zone 3)

Figure 2. SFDR vs f_{IN}

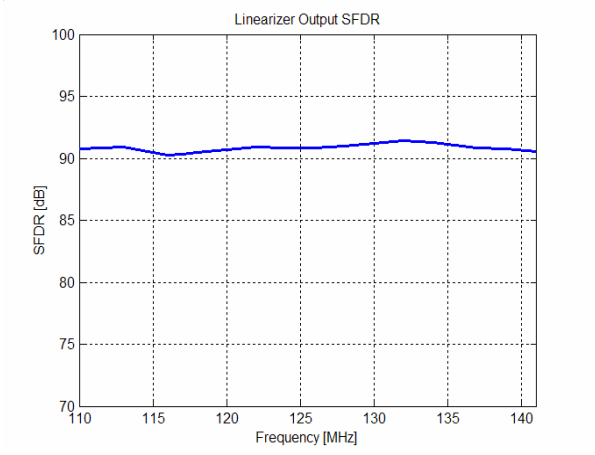


Figure 5. THD vs f_{IN}

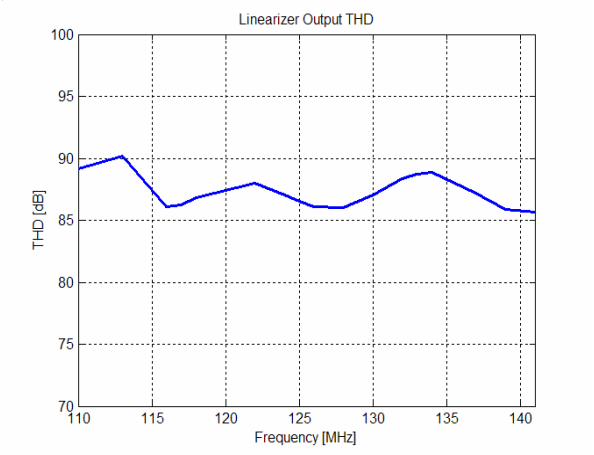


Figure 3. Single Tone (147.8MHz)
Before Linearization SFDR 62.9dB (typ)

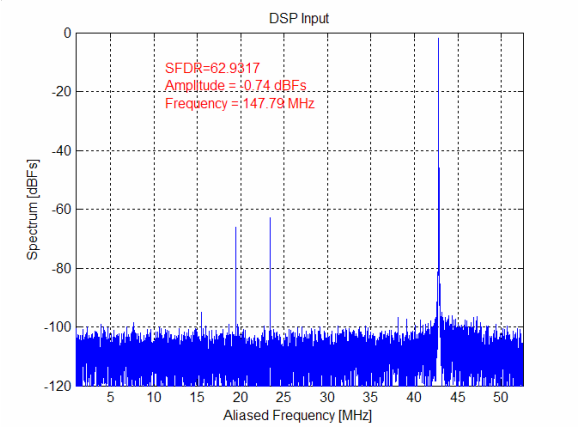


Figure 6. Single tone (147.8MHz)
After Linearization SFDR 92.6dB (typ)

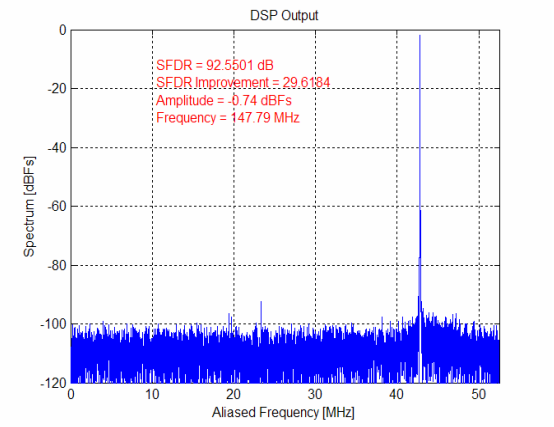


Figure 4. Two Tone (110.7, 116.8MHz)
Before Linearization SFDR 73.8dB (typ)

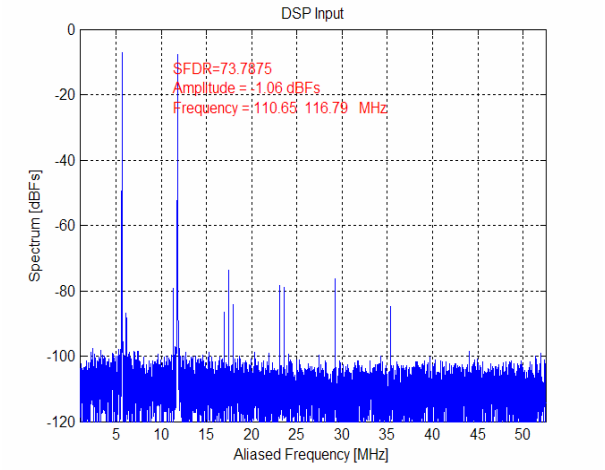


Figure 7. Two Tones (110.7, 116.8MHz)
After Linearization SFDR 94.6dB (typical)

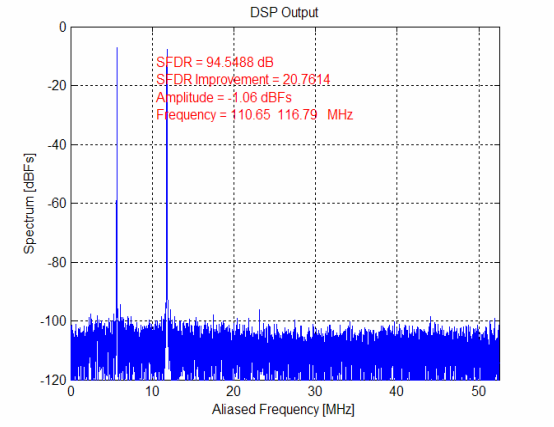


Figure 8. Three Tone (111.2, 115.0, 134.0MHz) Before Linearization SFDR 80.2dB (typ)

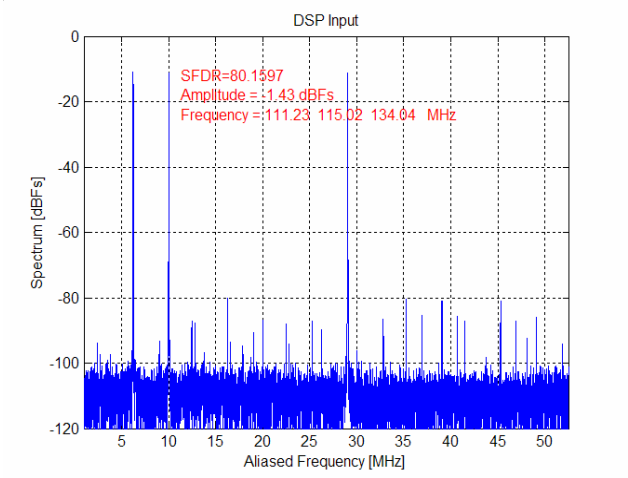


Figure 9. SNR vs F_{IN}

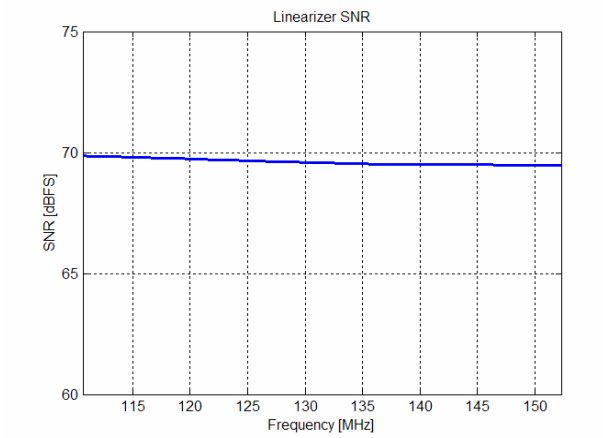
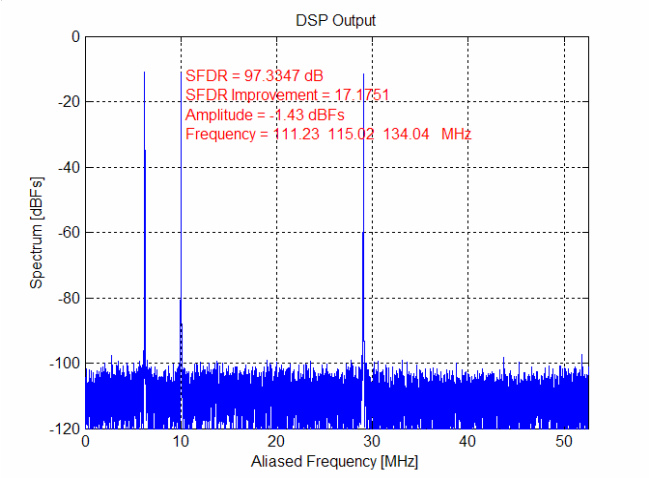


Figure 10. Three Tone (111.2, 115.0, 134.0MHz) Before Linearization SFDR 97.2 dB (typ)



Definition of Specifications

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay in time between the falling edge of the input sampling clock and the actual time at which sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Differential Input Voltage

The peak-to-peak differential voltage that must be applied to generate a full scale response. The peak differential voltage is calculated by measuring the voltage on one input pin and subtracting the voltage on the other input pin which is 180^{o} out of phase. The peak to peak value is then calculated by obtaining the voltages of the input pins with the phases reverses and calculating the difference between the peak measurements.

Differential Non Linearity (DNL)

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

An indication of the quality of an analog-to-digital converter. ENOB can be calculated with the following formula:

Equation 1. $$\mathrm{ENOB} = \frac{\mathrm{SINAD}-1.76}{6.02}$$

Gain Error

The amount of deviation (expressed in dB) between the nominal input signal required to achieve -1dBFS at the mid-point frequency of the Nyquist Zone and the measured input signal power to achieve -1dBFS at any given frequency in the specified Nyquist Zone.

Integral Non Linearity (INL)

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a linear least squares curves fit.

Maximum Conversion Rate

The clock rate at which parametric testing is performed.

Minimum Conversion Rate

The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Nyquist Zone

The product performance is specified for input frequencies in three Nyquist zones. Typical performance is delivered over the middle 80% of each Nyquist zone.

- Nyquist Zone 1: 0 - $f_{s/2}$
- Nyquist Zone 2: $f_{s/2}$ - f_s
- Nyquist Zone 3: f_s - $3f_{s/2}$
- Nyquist Zone 4: $3f_{s/2}$ - $2f_s$
- Nyquist Zone 5: $2f_s$ - $5f_{s/2}$

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power Supply Rejection

The change in full scale from the value with the supply at the minimum limit to the value with the supply at the maximum limit measured at the mid-band frequency of the Nyquist zone under test.

Propagation Delay

The delay between the input clock rising edge and the time when all data bits are within valid logic levels.

Signal-to-Noise and Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic.

Temperature Drift

As measured for offset or gain error, it specifies the maximum change from the initial temperature value to the value at T_{Min} or T_{Max}.

Total Harmonic Distortion (THD)

The ratio of the rms signal amplitude of the input to the rms value of distortion appearing at multiples (harmonics) of the input.

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR

The ratio of the rms full scale input to the rms value of the peak spurious component which may or may not be an IMD product.

Theory of Operation

The OM1400A-105 is an analog-to-digital converter module with exceptional linearity. Its design provides the user with an ultra-low distortion digital output enabling high-performance applications in communications, test and measurement, medical imaging, scientific and industrial markets.

The module is comprised of a high-performance AD8351 buffer amplifier, AD6645 14-bit high-speed analog-to-digital converter and Optichron's Linearizer with embedded Turbolinear™ technology. Optichron's Linearizer performs the signal linearization function.

Nonlinear distortion in analog-to-digital data conversion applications is generated in both the buffer amplifier and the analog-to-digital converter and results in undesired harmonics and inter-modulation products that degrade system performance. The phenomenon of nonlinear distortion is very difficult to overcome because its sources are modeled as higher-order mathematical functions that can have many shapes and forms. The resulting nonlinear signal interferes with the desired linear output. This interference is problematic as it can be continuous or discontinuous, static or dynamic as well as temperature-dependent.

Nonlinear distortion results in poor Spurious Free Dynamic Range (SFDR) and Total Harmonic Distortion (THD). Optichron's Linearizer operates on the digital output of the AD6645 to produce a linearized digital signal with a typical 25 dB improvement in SFDR and THD. Optichron's Linearizer does not affect the AD6645's output signal-to-noise ratio.

OM1400A-105 ADC Module

The ADC, differential amplifier, Linearizer and the supporting components that constitute the module are assembled on a FR4 substrate that is 2.05" x 1.4" in dimension. The bottom of the module has a ball grid array with a pitch of 0.05". The module requires supply voltages of 5V (analog), 3.3V (digital) and 1.8V (I/Os).

At the input to the module is the AD8351, a low distortion, low noise differential amplifier that can be used in RF/IF applications up to 2.2GHz. The module presents a single-ended 50 ohm load to the driving circuit and hence needs to be driven from a source capable of delivering +4 dBm into 50 ohms. The AD8351 buffer amplifier converts the single-ended input to a differential signal to drive the AD6645 ADC directly. The buffer amplifier also provides gain, isolation, source matching and a balanced input to the AD6645 easing the drive requirements of the application circuit.

The AD6645 is a monolithic 14-bit 105 MSPS pipelined ADC with a typical SFDR of 89 dBc at 70 MHz f_{IN}. Due to the dynamic nature of the nonlinear effects at higher input frequencies and when a buffer amplifier is used to drive an ADC, the degradation in linearity is typically greater with the combination of the ADC and amplifier than with the ADC alone.

A differential 2.2 V_{P-P} is applied at the input of the ADC. Applying differential inputs provides a high common-mode rejection of stray signals such as local oscillator feed through, ground and power noise. The differential inputs help enhance AC performance at high sample rates and enable a very high usable input bandwidth which is important in undersampling applications.

Nonlinear distortion in a typical pipelined ADC arises from imbalances in component tolerances at many nodes in the pipe, as well as from the actual nonlinear nature of circuit elements such as amplifiers, resistors, capacitors or diode effects on the chip. Unlike noise effects, nonlinear effects are deterministic and reproducible and are a function of the input signal and some external variables such as the input impedance of the amplifier and the ADC, supply voltage and temperature.

The Linearizer with Turbolinear™ technology is a high-performance hard-wired signal processing engine customized to handle nonlinear filtering operations. The input to the Linearizer is the 14-bit parallel CMOS output of the AD6645. While the input to the AD6645 can be in the Nyquist zones 2, 3 or 4, the digital output is always aliased to baseband as dictated by sampling theory. The Linearizer performs nonlinear filtering operations in real-time on the output of the AD6645 and provides a linearized version. Typical improvements in SFDR are on the order of 25 dB.

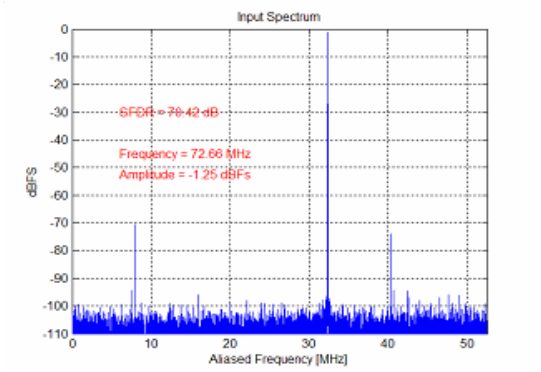
Nearly every element in the analog signal path can cause nonlinear distortion. However, distortion products grow progressively worse as the signal amplitude increases. In most applications the signal must be amplified significantly to drive the ADC input, causing the signal to reach its maximum amplitude at the input of the ADC. Therefore the ADC and buffer amplifier typically contribute the most distortion, limiting the overall system linearity. The Linearizer is able to remove the nonlinear distortion associated with these two components, thereby eliminating a primary bottleneck to building highly linear systems. By including a buffer amplifier with gain, the full scale power required to drive the OM1400A-105 is reduced, easing the burden of maintaining high linearity in the rest of the system.

The following sections illustrate the performance of the differential amplifier and ADC combination before and after the Linearization process.

Performance Prior to Linearization

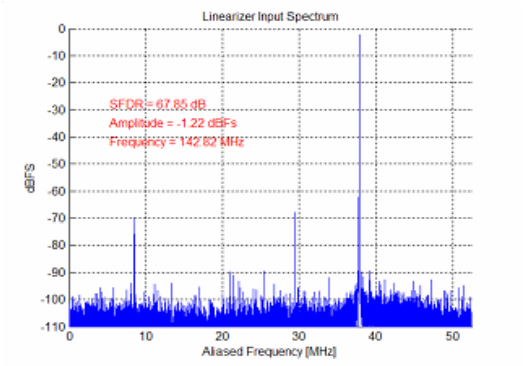
For a single tone at 72.7MHz, in the 2nd Nyquist zone at an amplitude -1.25 dBFS the typical SFDR at the output of the amplifier and ADC combination is 70.4dB.

Figure 11. Single Tone at 72.7MHz, 70.4dB (typ)



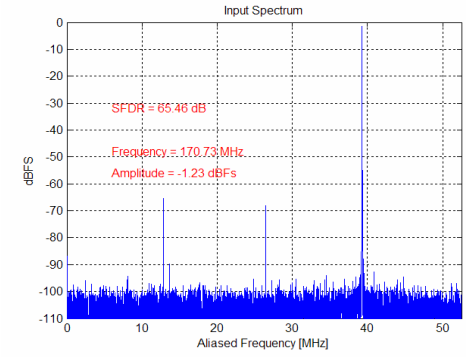
For a single tone at 142.9MHz, in the 3rd Nyquist zone at an amplitude -1.22 dBFS the typical SFDR at the output of the amplifier and ADC combination is 67.9dB.

Figure 12. Single Tone at 142.7MHz, 67.8dB (typ)



For a single tone at 170.7MHz, in the 4th Nyquist zone at an amplitude -1.23 dBFS the typical SFDR at the output of the amplifier and ADC combination is 65.5dB.

Figure 13. Single Tone at 170.7MHz, SFDR 65.5dB

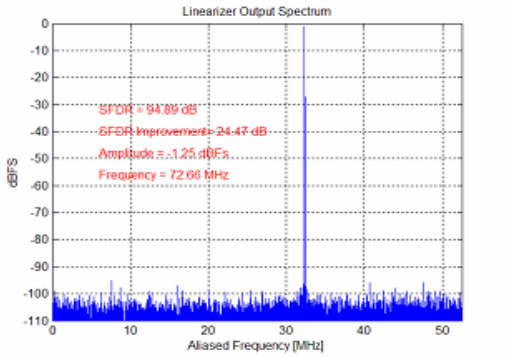


As illustrated above, the signal degradation due to nonlinear distortion progressively increases in the higher Nyquist zones.

Performance After Linearization

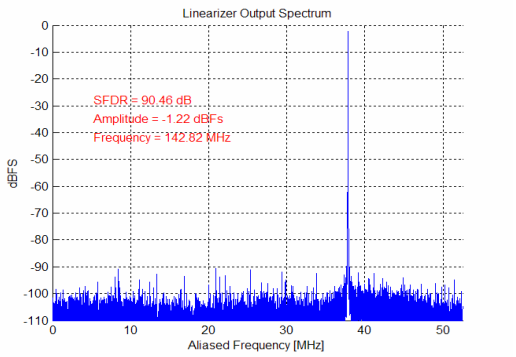
In the 2nd Nyquist zone, the SFDR upon linearization is around 94.9dB typical, a 25dB improvement.

Figure 14. Single Tone at 72.7MHz, SFDR 94.9dB (typ)



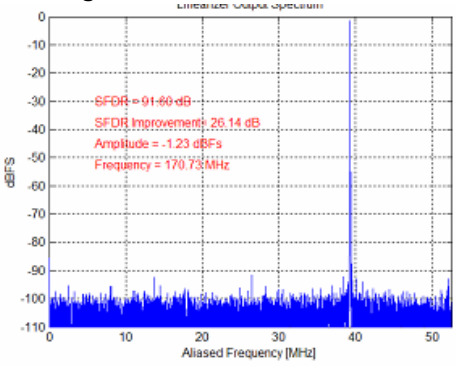
In the 3rd Nyquist zone, the SFDR upon linearization is around 90.5dB typical, a 22dB improvement.

Figure 15. Single Tone at 142.73 MHz, 90.5dB (typ)



In the 4th Nyquist zone, the SFDR upon linearization is around 91.6dB typical, a 26 dB improvement.

Figure 16. Single Tone at 170.7MHz, SFDR 91.6dB



As shown in the plots above, the linearizer effectively cancels nonlinear distortion in the relevant Nyquist zone enhancing the linearity of the ADC and amplifier combination.

System Benefits

High linearity enabled by the Linearizer with embedded-Turbolinear™ technology offers several benefits in various applications.

In IF sampling receivers, the Linearizer enables the sampling of signals at higher IF thus resulting in the elimination of an IF stage. This reduces component count, board area, filtering requirements, power dissipation, and system cost while improving overall system reliability.

IF receivers using a single IF stage, the Linearizer allows the use of low power buffer amplifiers while enhancing the linearity and reducing system power consumption.

The improvement in SFDR that the Linearizer provides helps a receiver discern a weak signal in the presence of a strong interfering signal that otherwise would not be recovered.

In wide band RF receiver applications, the nonlinearities of the ADC and buffer amplifier introduce intermodulation (IMD) products between different channels. This forces the use of separate filters and ADCs for each channel. Optichron's Linearizer allows a single receive path to handle multiple channels by eliminating the nonlinear distortion and IMD products.

In test and measurement equipment, the Linearizer enables highly linear digitized signal capture. This allows for better characterization of high-speed mixed-signal products.

Applications Information

Clock Input

The user should make sure that the clock input signal is of high quality; a low jitter, low phase noise source is required to ensure optimal performance. Additionally, in order to keep the accuracy of the 14-bit conversion, there is a requirement to drive the clock inputs differentially and to have the input signal AC coupled to the ClkInN and ClkInP clock inputs. For a single-ended sinusoidal reference signal, the conversion to differential can be done with a transformer like the ADT4-1WT. Figure 17 shows a typical circuit where the clock is transformed from single-ended to differential using an RF transformer. It is recommended that the single-ended sinusoid have a signal power of at least 13 dBm for best performance. Narrow band-pass filtering of this sinusoid will help reduce the jitter on this reference. The Schottky diodes across the secondary of the transformer limits the noise into the clock input pins and limits the voltage swing at the rails. It is important that the differential clock signal lines be placed closely together and that they are isolated from other analog inputs and from digital outputs. This is the circuit used on the OM1400A-105 Evaluation Board. Alternately, a low-jitter differential ECL/PECL clock signal may be AC coupled with series capacitors to the ClkInP and ClkInN inputs.

Analog Input

The module provides a 50 ohm load AC input impedance, therefore the user needs to provide a single-ended analog input source capable of driving 50 Ohms at 4 dBm to achieve full-scale. The module uses an AD8351 RF Amplifier to convert the single-ended analog input to a differential pair that drives the AD6645 AIn and AIn_n inputs as shown in Figure 18. The module AIn input signal is AC coupled to to the InHi input of the AD6645 while the InLo input is AC coupled to ground. R24 is used as a feedback resistor to balance the differential outputs and R23 is used to set the gain.

Figure 17. Single-Ended to Differential Clock Input

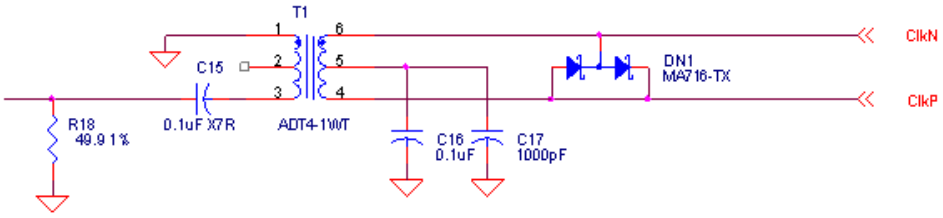
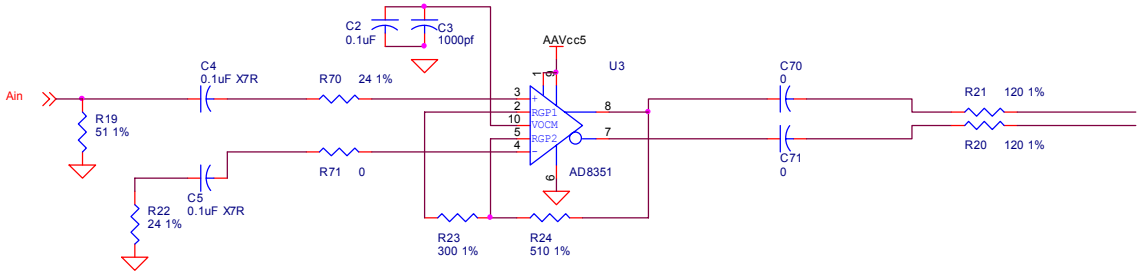


Figure 18. Single-Ended to Differential Analog Input



Supplies and By-passing

Power supply characteristics are important in high performance analog-to-digital converters. It is recommended that linear power supplies be used or if switching power supplies are used that they are appropriately shielded and filtered to avoid introducing spurious signals into the ADC. Both the 3.3V and 5.0V supplies should be turned on simultaneously. The power on rise time of the power supplies should be less than 45ms. Decoupling capacitors need to be positioned as close to each power pins as possible to minimize high frequency supply noise by satisfying local current demands. It is recommended to use 10%, 16V X7R 0603 0.1 uF and 20%,10V X7R 1206 10uF capacitors for optimal results with the 0.1 uF being the closest to the pin.

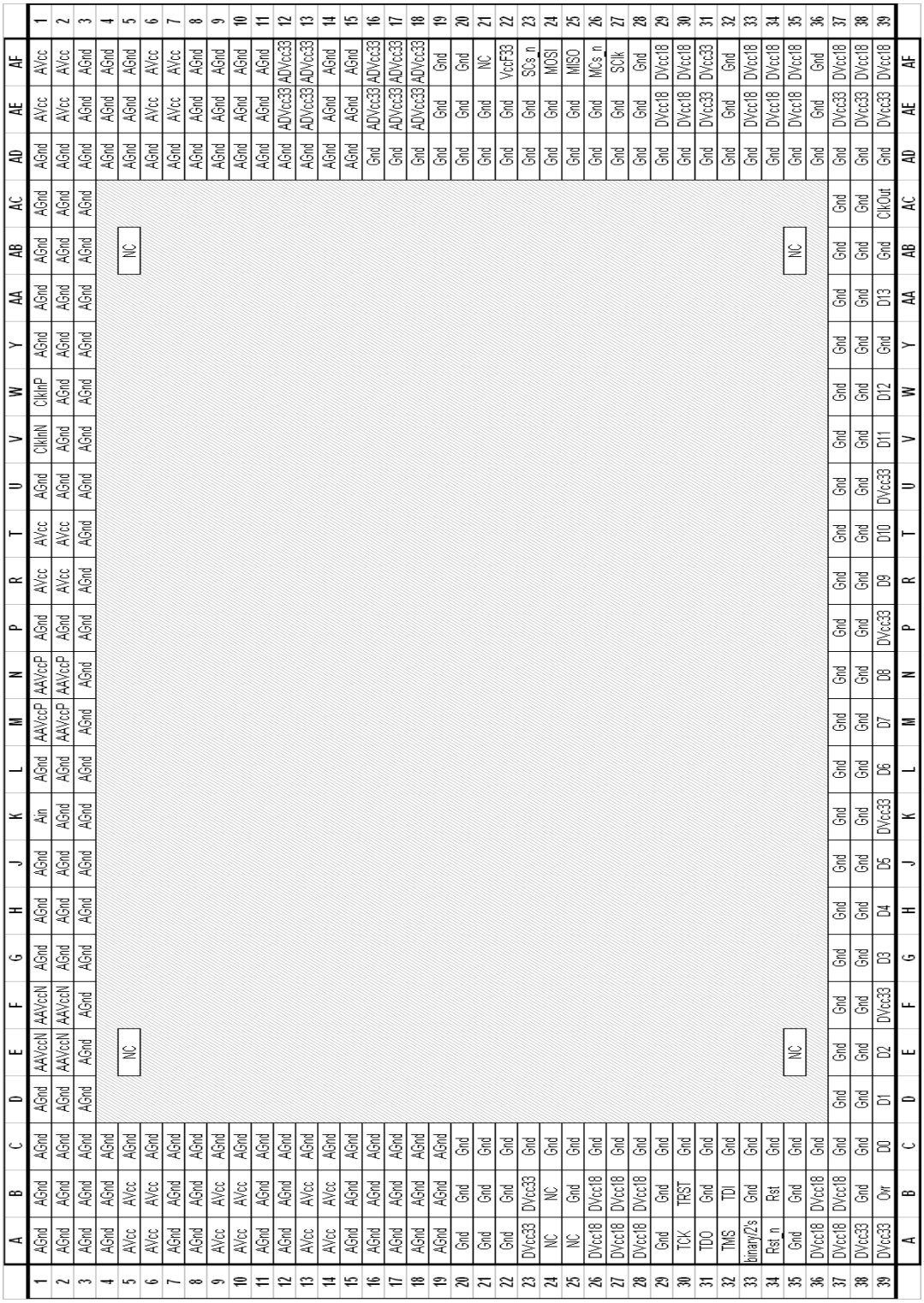
Grounding

To minimize the chance of digital switching creating current coupling into analog ground, the recommendation is to use a multi-layer board with a single ground plane. It is also necessary to ensure that the digital and analog sections are kept physically apart from each other and that digital traces are not routed near or under unshielded analog lines. The ADC module pin-out is such that this can be straightforward. The ball rows 1-19 on the top side of the module are allocated to analog functions, power and ground and the ball rows from 20-39 on the bottom side are all allocated to digital functions, power and ground.

Digital Outputs

There are 13 data output pins that provide the digital output from the Linearizer. The format of that output (binary or 2s complement) is selected via the Binary/2s input. The port is a standard 8-mA, 3.3V CMOS output. Therefore, the digital outputs should be routed to minimize capacitive loading and fan out (it is recommended to use only one gate on each output line); for example, to maintain a 2-ns edge, the total capacitance on a given output line should not exceed 5 pF. Digital output timing is maintained for loads up to 10 pF provided the capacitive loading on data and clock lines are well matched. External series resistors on the output lines are included inside the module and are not required on the board to which the module attaches.

Pin Configuration Top View



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
1	AGnd	AGnd	AGnd	AGnd	AAVccN	AAVccN	AGnd	AGnd	AGnd	Ain	AGnd	AAVccP	AAVccP	AGnd	AVcc	AVcc	AGnd	ClkInN	ClkInP	AGnd	AGnd	AGnd	AGnd	AGnd	AVcc	AVcc	1
2	AGnd	AGnd	AGnd	AGnd	AAVccN	AAVccN	AGnd	AGnd	AGnd	AGnd	AGnd	AAVccP	AAVccP	AGnd	AVcc	AVcc	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AVcc	AVcc	2
3	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	3
4	AGnd	AGnd	AGnd																					AGnd	AGnd	AGnd	4
5	AVcc	AVcc	AGnd		NC																	NC		AGnd	AGnd	AGnd	5
6	AVcc	AVcc	AGnd																					AGnd	AVcc	AVcc	6
7	AGnd	AGnd	AGnd																					AGnd	AVcc	AVcc	7
8	AGnd	AGnd	AGnd																					AGnd	AGnd	AGnd	8
9	AVcc	AVcc	AGnd																					AGnd	AGnd	AGnd	9
10	AVcc	AVcc	AGnd																					AGnd	AGnd	AGnd	10
11	AGnd	AGnd	AGnd																					AGnd	AGnd	AGnd	11
12	AGnd	AGnd	AGnd																					AGnd	ADVcc33	ADVcc33	12
13	AVcc	AVcc	AGnd																					AGnd	ADVcc33	ADVcc33	13
14	AVcc	AVcc	AGnd																					AGnd	AGnd	AGnd	14
15	AGnd	AGnd	AGnd																					AGnd	AGnd	AGnd	15
16	AGnd	AGnd	AGnd																					Gnd	ADVcc33	ADVcc33	16
17	AGnd	AGnd	AGnd																					Gnd	ADVcc33	ADVcc33	17
18	AGnd	AGnd	AGnd																					Gnd	ADVcc33	ADVcc33	18
19	AGnd	AGnd	AGnd																					Gnd	Gnd	Gnd	19
20	Gnd	Gnd	Gnd																					Gnd	Gnd	Gnd	20
21	Gnd	Gnd	Gnd																					Gnd	Gnd	NC	21
22	Gnd	Gnd	Gnd																					Gnd	Gnd	VccF33	22
23	DVcc33	DVcc33	Gnd																					Gnd	Gnd	SCs_n	23
24	NC	NC	Gnd																					Gnd	Gnd	MOSI	24
25	NC	Gnd	Gnd																					Gnd	Gnd	MISO	25
26	DVcc18	DVcc18	Gnd																					Gnd	Gnd	MCs_n	26
27	DVcc18	DVcc18	Gnd																					Gnd	Gnd	SClk	27
28	DVcc18	DVcc18	Gnd																					Gnd	Gnd	Gnd	28
29	Gnd	Gnd	Gnd																					Gnd	DVcc18	DVcc18	29
30	TCK	TRST	Gnd																					Gnd	DVcc18	DVcc18	30
31	TDO	Gnd	Gnd																					Gnd	DVcc33	DVcc33	31
32	TMS	TDI	Gnd																					Gnd	Gnd	Gnd	32
33	binary/2's	Gnd	Gnd																					Gnd	DVcc18	DVcc18	33
34	Rst_n	Rst	Gnd																					Gnd	DVcc18	DVcc18	34
35	Gnd	Gnd	Gnd		NC																	NC		Gnd	DVcc18	DVcc18	35
36	DVcc18	DVcc18	Gnd																					Gnd	Gnd	Gnd	36
37	DVcc18	DVcc18	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	DVcc33	DVcc18	37
38	DVcc33	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	DVcc33	DVcc18	38
39	DVcc33	Cwr	D0	D1	D2	DVcc33	D3	D4	D5	DVcc33	D6	D7	D8	DVcc33	D9	D10	DVcc33	D11	D12	Gnd	D13	Gnd	ClkOut	Gnd	DVcc33	DVcc18	39
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	

Pin Assignments

Table 8: Pin Assignments by Function

Function	Ball Number	Signal Name
Active High Reset	B34	RST_N
Active Low Reset	A34	RST (NC on this module)
Amplifier Positive Supply Voltage	M1, M2, N1, N2	AAV_{CCP}
Amplifier Negative Supply Voltage (Linearized ADC Module standard family pinout; not required for the OM1400A-105)	E1, E2, F1, F2,	AAV_{CCN}
Analog Ground	A1-4, A7-8, A11-12, A15-19, B1-4, B7-8, B11-12, B15-19, C1-19, D1-3, E3, F3, G1-3, H1-3, J1-3, K2-3, L1-3, M3, N3, P1-3, R3, T3, U1-3, V2-3, W2-3, Y1-3, AA1-3, AB1-3, AC1-3, AD1-15, AE3-6, AE8-11, AE14-15, AF3-6, AF8-11, AF14-15	AGND
Analog Input Signal	K1	AIN
Clock Input Negative. Complement of ClkInP, Differential Input.	W1	CLKINN
Clock Input Positive. Conversion on Rising Edge.	V1	CLKINP
Clock Output of Linearizer	AC39	CLKOUT
Core Analog Supply for ADC	A5-6, A9-10, A13-14, B5-6, B9-10, B13-14, R1-2, T1-2, AE1-2, AE6-7, AF1-2, AF6-7	AV_{CC}
Core Supply for Linearizer	A26-28, A36-37, B26-28, B36-37, AE29-30, AE33-35, AF29-30, AF33-35, AF37-39	DV_{CC18}
Data Output of Linearizer in 2s Complement if binary/2s is set.	C39, D39, E39, G39, H39, J39, L39, M39, N39, R39, T39, V39, W39, AA39	D(0-13)
Digital Ground	A20-22, A29, A35, B20-22, B29, B35, B38, C20-38, D37-38, E37-38, F37-38, G37-38, H37-38, J37-38, K37-38, L37-38, M37-38, N37-38, P37-38, R37-38, T37-38, U37-38, V37-38, W37-38, Y37-39, AA37-38, AB37-39, AC37-38, AD16-39, AF19-28, AF32, AF36	GND
Digital I/O Supply for ADC	AE12-13, AE16-18, AF12-13, AF16-18	ADV_{CC33}
Flash Memory Supply Voltage	AF22	V_{CCF33}
I/O Supply for Linearizer	A23, A38-39, B23, F39, K39, P39, U39, AE31, AE37-39, AF31	DV_{CC33}
JTAG	B30	TRST
JTAG	A30	TCK
JTAG	A31	TDO
JTAG	A32	TMS
JTAG	B32	TDI
No Connect	A24, A25, B24, E5, E35, AB5, AB35, AF21, AF23	NC
Set 2s Complement Output. Reset Binary Output.	A33	Binary/2s

Table 8: Pin Assignments by Function (Continued)

Function	Ball Number	Signal Name
Serial Peripheral Interface	AF23	SCS_N
Serial Peripheral Interface	AF24	MOSI
Serial Peripheral Interface	AF25	MISO
Serial Peripheral Interface	AF26	MCS_N
Serial Peripheral Interface	AF27	SCLK

Table 9: Pin Assignments by Pin Number

Pin Number	Signal
A1	AGND
A2	AGND
A3	AGND
A4	AGND
A5	AVCC33
A6	AVcc33
A7	AGND
A8	AGND
A9	AVcc33
A10	AVcc33
A11	AGND
A12	AGND
A13	AVcc33
A14	AVcc33
A15	AGND
A16	AGND
A17	AGND
A18	AGND
A19	AGND
A20	GND
A21	GND
A22	GND
A23	DVCC33
A24	NC
A25	NC
A26	DVCC18
A27	DVCC18

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
A28	DVCC18
A29	GND
A30	TCK
A31	TDO
A32	TMS
A33	BINARY 2S
A34	NC (RST)
A35	GND
A36	DVCC18
A37	DVCC18
A38	DVCC33
A39	DVCC33
B1	AGND
B2	AGND
B3	AGND
B4	AGND
B5	AVcc33
B6	AVcc33
B7	AGND
B8	AGND
B9	AVcc33
B10	AVcc33
B11	AGND
B12	AGND
B13	AVcc33
B14	AVcc33
B15	AGND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
B16	AGND
B17	AGND
B18	AGND
B19	AGND
B20	GND
B21	GND
B22	GND
B23	DVCC33
B24	NC
B25	GND
B26	DVCC18
B27	DVCC18
B281	DVCC18
B29	GND
B30	TRST
B31	GND
B32	TDI
B33	GND
B34	RST_N
B35	GND
B36	DVCC18
B37	DVCC18
B38	GND
B39	NC
C1	AGND
C2	AGND
C3	AGND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
C4	AGND
C5	AGND
C6	AGND
C7	AGND
C8	AGND
C9	AGND
C10	AGND
C11	AGND
C12	AGND
C13	AGND
C14	AGND
C15	AGND
C16	AGND
C17	AGND
C18	AGND
C19	AGND
C20	GND
C21	GND
C22	GND
C23	GND
C24	GND
C25	GND
C26	GND
C27	GND
C28	GND
C29	GND
C30	GND
C31	GND
C32	GND
C33	GND
C34	GND
C35	GND
C36	GND
C37	GND
C38	GND
C39	D0

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
D1	AGND
D2	AGND
D3	AGND
D37	GND
D38	GND
D39	D1
E1	AAVCCN
E2	AAVCCN
E3	AGND
E37	GND
E38	GND
E39	D2
F1	AAVCCN
F2	AAVCCN
F3	AGND
F37	GND
F38	GND
F39	DVCC33
G1	AGND
G2	AGND
G3	AGND
G37	GND
G38	GND
G39	D3
H1	AGND
H2	AGND
H3	AGND
H37	GND
H38	GND
H39	D4
J1	AGND
J2	AGND
J3	AGND
J37	GND
J38	GND
J39	D5

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
K1	AIN
K2	AGND
K3	AGND
K37	GND
K38	GND
K39	DVCC33
L1	AGND
L2	AGND
L3	AGND
L37	GND
L38	GND
L39	D6
M1	AAVCC5
M2	AAVCC5
M3	AGND
M37	GND
M38	GND
M39	D7
N1	AAVCC5
N2	AAVCC5
N3	AGND
N37	GND
N38	GND
N39	D8
P1	AGND
P2	AGND
P3	AGND
P37	GND
P38	GND
P39	DVCC33
R1	AVcc33
R2	AVcc33
R3	AGND
R37	GND
R38	GND
R39	D9

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
T1	AVcc33
T2	AVcc33
T3	AGND
T37	GND
T38	GND
T39	D10
U1	AGND
U2	AGND
U3	AGND
U37	GND
U38	GND
U39	DVCC33
V1	CLKINN
V2	AVcc33
V3	AGND
V37	GND
V38	GND
V39	D11
W1	CLKINN
W2	AVcc33
W3	AGND
W37	GND
W38	GND
W39	D12
Y1	AGND
Y2	AGND
Y3	AGND
Y37	GND
Y38	GND
Y39	GND
AA1	AGND
AA2	AGND
AA3	AGND
AA37	GND
AA38	GND
AA39	D13

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
AB1	AGND
AB2	AGND
AB3	AGND
AB37	GND
AB38	GND
AB39	GND
AC1	AGND
AC2	AGND
AC3	AGND
AC37	GND
AC38	GND
AC39	CLKOUT
AD1	AGND
AD2	AGND
AD3	AGND
AD4	AGND
AD5	AGND
AD6	AGND
AD7	AGND
AD8	AGND
AD9	AGND
AD10	AGND
AD11	AGND
AD12	AGND
AD13	AGND
AD14	AGND
AD15	AGND
AD16	GND
AD17	GND
AD18	GND
AD19	GND
AD20	GND
AD21	GND
AD22	GND
AD23	GND
AD24	GND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
AD25	GND
AD26	GND
AD27	GND
AD28	GND
AD29	GND
AD30	GND
AD31	GND
AD32	GND
AD33	GND
AD34	GND
AD35	GND
AD36	GND
AD37	GND
AD38	GND
AD39	GND
AE1	AVcc33
AE2	AVcc33
AE3	AGND
AE4	AGND
AE5	AGND
AE6	AVcc33
AE7	AVcc33
AE8	AGND
AE9	AGND
AE10	AGND
AE11	AGND
AE12	ADVCC33
AE13	ADVCC33
AE14	AGND
AE15	AGND
AE16	ADVCC33
AE17	ADVCC33
AE18	ADVCC33
AE19	GND
AE20	GND
AE21	GND

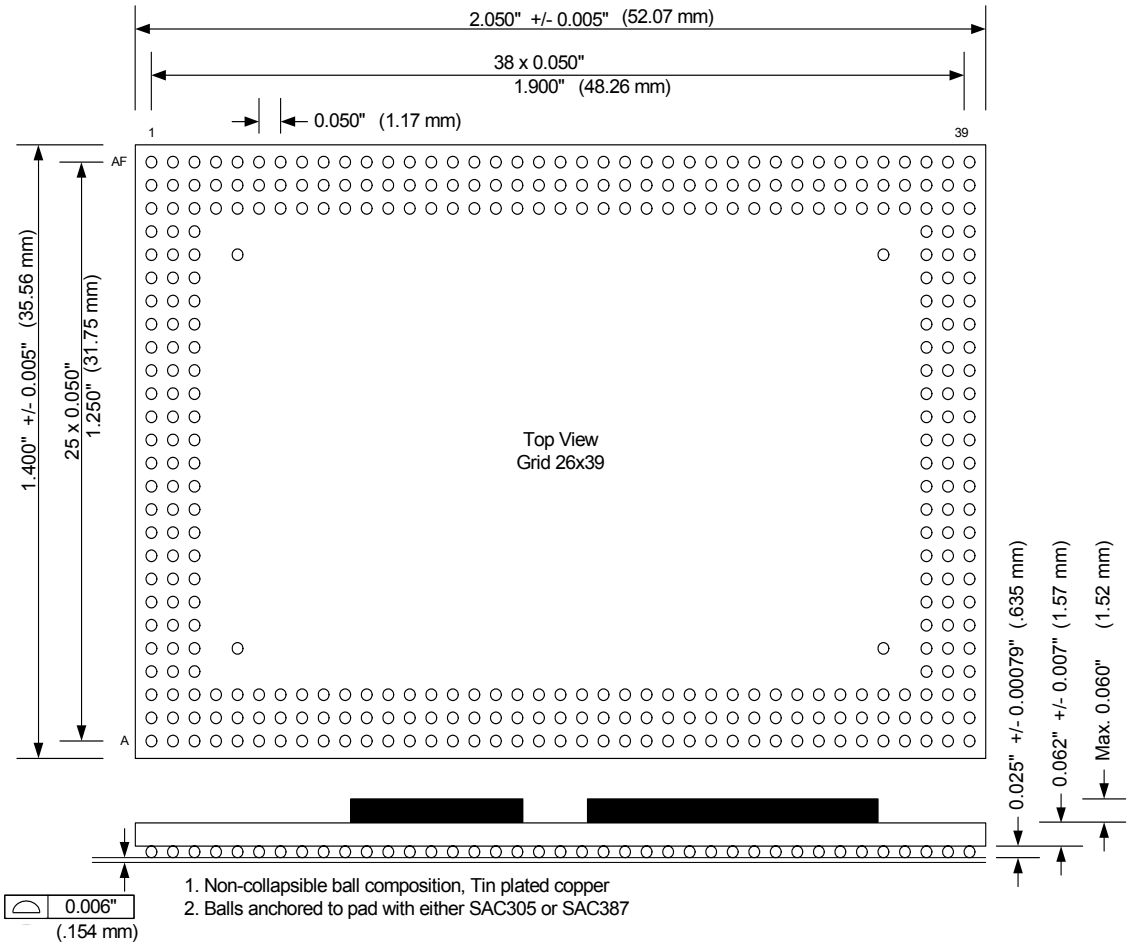
Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
AE22	GND
AE23	GND
AE24	GND
AE25	GND
AE26	GND
AE27	GND
AE28	GND
AE29	DVCC18
AE30	DVCC18
AE31	DVCC33
AE32	GND
AE33	DVCC18
AE34	DVCC18
AE5	DVCC18
AE36	GND
AE37	DVCC33
AE38	DVCC33
AE39	DVCC33
AF1	AVcc33
AF2	AVcc33
AF3	AGND
AF4	AGND
AF5	AGND
AF6	AVcc33
AF7	AVcc33
AF8	AGND
A9	AGND
AF10	AGND
AF11	AGND
AF12	ADVCC33
AF13	ADVCC33
AF14	AGND
AF15	AGND
AF16	ADVCC33
AF17	ADVCC33
AF18	ADVCC33

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
A19	GND
AF20	GND
AF21	NC
AF22	VCCF33
AF23	SCS_N
AF24	MOSI
AF25	MISO
AF26	MCS_N
AF27	SCLK
AF28	GND
AF29	DVCC18
AF30	DVCC18
AF31	DVCC33
AF32	GND
AF33	DVCC18
AF34	DVCC18
AF35	DVCC18
AF36	GND
AF37	DVCC18
AF38	DVCC18
AF39	DVCC18

Mechanical Dimensions



Ordering Guide

Optichron's OM1400A-105 ADC module is available in different versions depending on the desired Nyquist zone of operation and desired sampling frequency. The Linearizer is programmed to cancel nonlinear distortion in the desired combination of Nyquist zone and sampling frequency. When ordering, the user must specify the Nyquist zone in which the input signal will fall for the desired sampling frequency.

Table 10: Ordering Guide

Product	Ordering Number	Sampling rate (MSPS)	Nyquist Zone
Linearized ADC Module			
OM1400A-105	OM1400A-1050NZ2	105.0	2
OM1400A-105	OM1400A-1050NZ3	105.0	3
OM1400A-105	OM1400A-1050NZ4	105.0	4
OM1400A-105	OM1400A-1000NZ2	100.0	2
OM1400A-105	OM1400A-1000NZ3	100.0	3
OM1400A-105	OM1400A-1000NZ4	100.0	4
OM1400A-105	OM1400A-0950NZ2	95.0	2
OM1400A-105	OM1400A-0950NZ3	95.0	3
OM1400A-105	OM1400A-0950NZ4	95.0	4
OM1400A-105	OM1400A-0900NZ2	90.0	2
OM1400A-105	OM1400A-0900NZ3	90.0	3
OM1400A-105	OM1400A-0900NZ4	90.0	4
Evaluation Board			
	OM1400A-1050NZ2EVAL	105.0	2
	OM1400A-1050NZ3EVAL	105.0	3
	OM1400A-1050NZ4EVAL	105.0	4
	OM1400A-1000NZ2EVAL	100.0	2
	OM1400A-1000NZ3EVAL	100.0	3
	OM1400A-1000NZ4EVAL	100.0	4
	OM1400A-0950NZ2EVAL	95.0	2
	OM1400A-0950NZ3EVAL	95.0	3
	OM1400A-0950NZ4EVAL	95.0	4
	OM1400A-0900NZ2EVAL	90.0	2
	OM1400A-0900NZ3EVAL	90.0	3
	OM1400A-0900NZ4EVAL	90.0	4

Other bandwidths, offset intermediate frequencies, and other Nyquist zones are available upon request.

Please contact Optichron Sales for more information **510-249-5230** or **sales@optichron.com**.

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Revision History

Revision	Change	Page Number	Date
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